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Γ	APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
	10/073,442	02/11/2002	Robert Allan Whitton	0808.65530	4484
	24978 75	24978 7590 12/16/2005		EXAMINER	
	GREER, BUF	NS & CRAIN	TANG, KENNETH		
	300 S WACKER DR			ART UNIT	PAPER NUMBER
	25TH FLOOR CHICAGO, IL	CHICAGO, IL 60606			

DATE MAILED: 12/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

		Applicat	ion No.	Applicant(s)					
		10/073,4	142	WHITTON, ROB	WHITTON, ROBERT ALLAN				
Office Action Summary			er	Art Unit					
	·	Kenneth		2195					
Period fo	The MAILING DATE of this communica or Reply	ation appears on th	ie cover sheet v	vith the correspondence a	ddress				
WHIC - Exter after - If NO - Failu Any r	ORTENED STATUTORY PERIOD FOR CHEVER IS LONGER, FROM THE MAI resions of time may be available under the provisions of SIX (6) MONTHS from the mailing date of this community period for reply is specified above, the maximum statute to reply within the set or extended period for reply will eply received by the Office later than three months after adjustment. See 37 CFR 1.704(b).	LING DATE OF T 37 CFR 1.136(a). In no er ication. ory period will apply and v I, by statute, cause the ap	HIS COMMUN vent, however, may a will expire SIX (6) MO plication to become A	IICATION. a reply be timely filed ONTHS from the mailing date of this ABANDONED (35 U.S.C. § 133).					
Status									
1)⊠	Responsive to communication(s) filed on 19 September 2005.								
2a)⊠	This action is FINAL . 2b)☐ This action is	non-final.						
3)	Since this application is in condition fo	itters, prosecution as to th	ne merits is						
closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.									
Dispositi	on of Claims								
4)🖂	Claim(s) 1-15, 19, 27 and 30 is/are pend	ding in the applica	tion.						
	4a) Of the above claim(s) is/are withdrawn from consideration.								
5)	5) Claim(s) is/are allowed.								
6)⊠	☑ Claim(s) <u>1-9, 11-15,19,27 and 30</u> is/are rejected.								
•	Claim(s) <u>10</u> is/are objected to.								
8)∐	Claim(s) are subject to restriction	on and/or election	requirement.						
Applicat	on Papers								
9) The specification is objected to by the Examiner.									
10)[10) The drawing(s) filed on is/are: a) accepted or b) objected to by the Examiner.								
	Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).								
-	Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).								
11)	11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.								
Priority (ınder 35 U.S.C. § 119								
	12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) ■ All b) ■ Some * c) ■ None of: 1. ■ Certified copies of the priority documents have been received. 2. ■ Certified copies of the priority documents have been received in Application No								
	3. Copies of the certified copies of the priority documents have been received in this National Stage								
application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received.									
See the attached detailed Office action for a list of the certified copies flot received.									
Attachmen	t(s)								
	e of References Cited (PTO-892)			V Summary (PTO-413)					
3) 🔯 Infor	e of Draftsperson's Patent Drawing Review (PTC mation Disclosure Statement(s) (PTO-1449 or PT r No(s)/Mail Date <u>7/17/03</u> .			o(s)/Mail Date f Informal Patent Application (P ⁻ 	TO-152)				

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DETAILED ACTION

1. This action is in response to the Amendment filed on 9/19/05. Applicant's arguments have been fully considered are most in view of the new grounds of rejections.

2. Claims 1-15, 19, 27, and 30 are presented for examination.

Claim Objections

- 3. Claim 2 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. In claim 2, the limitation of an exception being generated to change from a first execution mode to a second execution mode is already introduced in claim 1.
- 4. Claim 8 is objected to because of the following informalities: The term "bared" is misspelled and grammatically incorrect. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

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5. Claims 1-9, 11, 13-14, 27, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zahir et al. (hereinafter Zahir) (US 6,065,114) in view of Rosenthal et al. (hereinafter Rosenthal) (US 5,127,098).

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- 6. As to claim 1, Zahir teaches a processor switchable between a first execution mode and a second execution mode (context switching between nodes), the processor having a first processor context (first context) when in the first execution mode and a second processor context (second context or target context), larger than (the context of BSPLOAD is smaller than PTR or the context of BSPLOAD is larger than PTR) the first processor context (context A compared to context B), when in the second execution mode, wherein the processor is arranged to execute a plurality of threads on a time share basis (concurrent processing or parallel), the threads being able to change (switching) execution mode, the processor is arranged to generate an exception (interrupt) when the processor attempts to change (switching) from one execution mode to the other to keep track (by using mode bits, etc.) of when the execution modes are used and control which processor contexts are preserved at which times (col. 8, lines 4-32 and lines 59-col. 9, lines 1-19, col. 10, lines 13-31, col. 11, lines 7-37, col. 1, lines 44-58, col. 14, lines 35-65, and claim 1,);
- 7. Zahir fails to explicitly teach wherein the number of threads in the second execution mode at any one time is limited, to limit the number of times that the second processor context is preserved and restored. However, Rosenthal teaches a time sharing technique such as priority scheduling for context switching, wherein the amount of context switching is limited (col. 7, lines 4-7, col. 4, lines 50-56, col. 11, lines 21-30, col. 1, lines 14-17, col. 4, lines 8-12). It would have been obvious to one of ordinary skill in the art at the time the invention was made to

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combine Zahir with Rosenthal because this would support context switching and minimize the overhead caused by context switching, thereby improving the system performance of a multitasking system (col. 4, lines 7-17).

- 8. As to claim 2, Zahir teaches wherein the exception (interrupt) is generated when the processor attempts to change from the first execution mode to the second execution mode (col. 8, lines 59- col. 9, lines 1-19, col. 10, lines 13-31, col. 11, lines 7-37, col. 1, lines 44-58, col. 14, lines 35-65, and claim 1).
- 9. As to claim 3, Zahir teaches wherein the processor is arranged to preserve the second processor context (store a content of a second register), or that part of the second processor context which is different from the first processor context, when said exception has been generated (interrupt from interrupt handler) (see Abstract, col. 1, lines 61-68 through col. 2, lines 1-10, col. 10, lines 13-31).
- 10. As to claim 4, Zahir teaches wherein the processor is arranged such that when the processor is switched to a thread which is in the first execution mode, or when the processor is switched to a thread which was the last thread to be in the second execution mode (context switching), and it is inherent that only the first processor context is preserved. Silberschatz's OPERATING SYSTEM CONCEPTS (4.2.3 Context Switch, page 97) shows that the standard definition of context switching requires saving the state of the old process and loading the saved state for the new process.

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11. As to claim 5, Zahir teaches wherein the second processor context, or that part of the second processor context which is different from the first processor context (context A compared to context B), preserved when the processor next enters the second execution mode to execute a thread other than the last thread to be in the second execution mode (second portion/content/register is reserved/saved/stored) (see Abstract and col. 1, lines 61-67 through col. 2, lines 1-8).

- 12. As to claim 6, it is inherent that Zahir teaches that the number of threads that may be in the second execution mode at any one time is less than the total number of threads that may be active on the processor at any one time because it is not possible for the number of threads in any mode to exceed the total number of threads.
- 13. As to claim 7, Zahir teaches wherein the processor is arranged such that, when said exception has been generated, a check is carried out to determine whether the thread that caused the exception is allowed to enter the second execution mode (the interrupt handler provides the controls for the interrupts) (col., 12, lines 22-36, etc.).
- 14. As to claim 8, Zahir teaches wherein the check comprises determining whether that thread is a thread which is barred (ignored or barred by the interrupt handler if the bit is not set) from the second execution mode (col. 11, lines 51-65).

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15. As to claim 9, Zahir teaches wherein the check (interrupt handler) comprises determining whether a predetermined number of other threads are already in the second execution mode (data table information) (col. 11, lines 7-22).

- 16. As to claim 11, Zahir teaches wherein the processor is arranged to execute a first instruction set when in the first execution mode and a second instruction set when in the second execution mode (see Abstract and col. 8, lines 4-32).
- As to claim 13, Zahir teaches the processor comprising at least one execution unit and a plurality of storage locations (backing store in memory and registers), the first processor context comprising the contents of storage locations accessible in first execution mode and the second processor context comprising the contents of storage locations (first register and second register) accessible in the second execution mode (see Abstract and col. 1, lines 61-67 through col. 2, lines 1-9).
- 18. As to claim 14, Zahir teaches the processor comprising a plurality of computational units for executing instructions in parallel, each computational unit having at least one execution unit and at least one storage location to which the execution unit has access (backing store in memory and registers) (col. 1, lines 44-58).
- 19. As to claims 27 and 30, they are rejected for the same reasons as stated in the rejection of claim 1.

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20. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zahir et al. (hereinafter Zahir) (US 6,065,114) in view of Rosenthal et al. (hereinafter Rosenthal) (US 5,127,098), and further in view of Ackerman et al. (hereinafter Ackerman) (US 5,481,719).

- As to claim 12, Zahir and Rosenthal fail to explicitly teach teaches wherein the processor is switchable between a supervisor mode and a user mode, the user mode having restricted access to the processor's resources in comparison to the supervisor mode, and, when said exception is generated, the processor transfers from the user mode to the supervisor mode. However, Ackerman teaches switching based on exceptions/interrupts between a supervisor mode and a user mode, whereby the user mode not having as much privileges as the supervisor mode (col. 20, lines 27-33, col. 13, lines 18-27). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the feature of the user mode and supervisor mode because the various levels of privileges increase the security of the system (col. 2, lines 23-25).
- Claims 15 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zahir et al. (hereinafter Zahir) (US 6,065,114) in view of Rosenthal et al. (hereinafter Rosenthal) (US 5,127,098), and further in view of Spiller (US 6,047,122).

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23. As to claim 15, Zahir and Rosenthal fail to explicitly teach wherein the first execution mode is a scalar mode and the second execution mode is a parallel mode. However, Spiller

teaches switching from a scalar mode to a parallel mode (col. 4, lines 1-17 and see claim 1). It

would have been obvious to one of ordinary skill in the art at the time the invention was made to

include the feature of switching from a scalar mode to a parallel mode because it would increase

the speed of processing (col. 2, lines 1-8).

24. As to claim 19, it is rejected for the same reasons as stated in the rejection of claim 15.

Allowable Subject Matter

25. Claim 10 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

26. Applicant's arguments in the Remarks have been fully considered but are now moot in view of the new grounds of rejections.

Conclusion

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Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth Tang whose telephone number is (571) 272-3772. The examiner can normally be reached on 8:30AM - 6:00PM, Every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kt 12/1/05

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